

CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:
2 a plurality of processors coupled together between which messages can be routed;
3 an I/O controller coupled to one or more of said processors;
4 at least one I/O device coupled to an I/O controller; and
5 wherein each processor is capable of detecting an error in a message sent from another
6 processor in the system and reformatting the message to indicate to other of said processors that the
7 message contains a transmission error.
- 1 2. The computer system of claim 1 wherein each of said messages between said processors
2 comprises multiple ticks, each tick comprising multiple bits of information, and wherein upon
3 detecting an error has occurred in a tick, the processor alters the tick in a predetermined manner to
4 indicate to other of said processors that the message contains an error.
- 1 3. The computer system of claim 1 wherein each of said messages between said processors
2 comprises multiple ticks, each tick comprising multiple bits of information including error check
3 bits, and wherein upon detecting an error has occurred in a tick, the processor alters the tick in a
4 predetermined manner to indicate to other of said processors that the message contains an error.
- 1 4. The computer system of claim wherein 1 wherein each of said messages between said
2 processors comprises multiple ticks, each tick comprising multiple bits of information, and wherein

3 upon detecting an error has occurred in a tick, the processor replaces the bits of information in the
4 tick with a predetermined bit pattern.

1 5. The computer system of claim 4 wherein said predetermined bit pattern includes a known
2 double bit error code.

1 6. The computer system of claim 1 wherein each of said messages between said processors
2 comprises multiple ticks, each tick comprising data bits and error check bits, and wherein upon
3 detecting an error has occurred in a tick, the processor replaces all of the bits in the tick with a
4 predetermined bit pattern.

1 7. The computer system of claim 6 wherein said predetermined bit pattern all 1's in place of
2 said data bits and an otherwise unused check bit code for said error check bits.

1 8. A processor, comprising:
2 a memory controller that coordinates transactions to a memory device; and
3 a router coupled to said memory controller and providing interfaces to one or more other
4 processors;
5 wherein said router is capable of detecting a transmission error in a message received from
6 another processor and reformatting the message to indicate that the message contains a
7 transmission error that has already been detected.

1 9. The processor of claim 8 wherein said message comprises multiple sequential blocks of
2 data, each data block comprising multiple bits of information, and wherein upon detecting that a
3 transmission error has occurred in a data block, the router alters the block in a predetermined
4 manner to indicate that the message contains a transmission error.

1 10. The processor of claim 8 wherein said message comprises multiple sequential blocks of
2 data, each data block comprising multiple bits of information including error check bits, and
3 wherein upon detecting that a transmission error has occurred in a data block, the router alters the
4 data block in a predetermined manner to that the message contains a transmission error.

1 11. The computer system of claim wherein 8 wherein said message comprises multiple
2 sequential blocks of data, each data block comprising multiple bits of information, and wherein
3 upon detecting that a transmission error has occurred in a data block, the router replaces the bits of
4 information in the data block with a predetermined bit pattern.

1 12. The computer system of claim 11 wherein said predetermined bit pattern includes a known
2 double bit error code.

1 13. The computer system of claim 8 said message comprises multiple sequential blocks of data,
2 each data block comprising data bits and error check bits, and wherein upon detecting that a
3 transmission error has occurred in a data block, the router replaces the all of the bits in the data
4 block with a predetermined bit pattern.

1 14. The computer system of claim 13 wherein said predetermined bit pattern includes all 1's in
2 place of said data bits and an otherwise unused check bit code for said error check bits.

1 15. A method of fault isolation in a multi-processor computer system, comprising:
2 (a) receiving a message;
3 (b) detecting an error in said message;
4 (c) replacing the erroneous portion of said message with a predetermined bit pattern to
5 indicate to other processors in said system that an error has occurred in said message and said error
6 has already been detected; and
7 (d) transmitting the message to another processor in said system.

1 16. The method of claim 15 wherein said message includes a data portion and an associated
2 error code portion and (c) includes replacing said data portion with all 1's and replacing said error
3 code portion with an otherwise unused value.

1 17. The method of claim 15 further including:
2 (e) alerting the system that a fault has been detected in said message.

1 18. The method of claim 17 further including:
2 (f) receiving said message that has been altered in (c);
3 (g) determining whether said message includes said predetermined bit pattern; and
4 (h) if said message includes said predetermines bit pattern, not alerting the system that
5 a fault is present in said message.

1 19. The method of claim 18 further including:

2 (i) transmitting said message with said predetermined bit pattern to another processor
3 in said system.

1 20. The method of claim 15 further including:

2 (j) receiving said message that has been altered in (c);

3 (k) determining whether said message includes said predetermined bit pattern; and

4 (l) if said message includes said predetermines bit pattern, not alerting the system that
5 a fault is present in said message.

1 21. The method of claim 20 further including:

2 (m) transmitting said message with said predetermined bit pattern to another processor
3 in said system.